REMARKS

Claims 1-11 have been pending in the application, of which claims 1-3, 6-7 and 9-11 have been rejected and claims 4-5 and 8 have been withdrawn from consideration. The Examiner is respectfully requested to reconsider and withdraw the rejection(s) and objection(s) in view of the amendments and remarks contained herein.

New claims 12-14 are added. These claims each depend from multiple dependent claim 6. The requisite fee for fifteen (15) new dependent claims ($270) is submitted herewith by check.

Claims 1, 2, 10 and 11 have been amended. However, the amendment to these claims merely correct grammatical or typographical errors. The scope of the original claims has not been changed and remains the same.

In the Action, the Examiner objected to the drawings under 37 C. F. R. 1.83 (a) for reason that the amplifier with a gate (claim 10), and the dual amplifier (claim 11) are not shown in the drawings. Claim 11 is drawn to a preferred embodiment shown in Figures 12 and 13, including the "bipolar" transistor (1303/ in Figure 12), rather than a dual amplifier as indicated by the Examiner. Claim 10 is drawn to a similar, but even more general embodiment including a field effect transistor (FET) instead of a bipolar transistor as recited in claim 11. Figure 12 was revised to include Figures 12a and 12b using a bipolar transistor 1303 and a FET 1303′ respectively. In view of the foregoing explanation, the objection to the drawings is submitted as overcome without need for amendment of any particular drawing.

REJECTIONS UNDER 35 U. S. C. §§ 102 AND 103

Claims 1, 2, 3, 6, 7 and 9 were rejected under 35 U. S. C. § 102 (b) as allegedly anticipated by Miguelez et al. (U.S. Patent No. 6,107,877). Claims 10 and 11 were rejected

under 35 U.S.C. § 103 (a) as allegedly unpatentable over Miguelez (previous cite) in view of Yun et al. (U.S. Patent No. 5,914,641) and Fukuden (U. S. Patent No. 5,805,023).

The aforementioned rejections are respectfully traversed without change to the scope of any of the original claims.

The claimed invention is patentably distinct from Miguelez et al. Claim 1 describes that a specific-frequency suppressing means is connected to one side or both sides of a nonlinear device directly, without another intervening device. The specific-frequency suppressing means is defined as suppressing all or part of the frequencies that are (in a range) from a frequency corresponding to DC, to a frequency corresponding to an occupied bandwidth of an input signal inputted to the input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of the input signal. Claim 2 goes on to detail that the impedance of the specific-frequency suppressing, as viewed from the connection point to which the specific-frequency suppressing means is connected, is lower than the impedance of the nonlinear device as viewed from the connection point at all or part of such aforementioned frequency range and/or high harmonic frequency.

Miguelez does not disclose the aforementioned claimed features of the frequency suppressing means to those of ordinary skill in the art. According to Applicants, resistors 106 and 112 (see Figure 6 of Miguelez) result in an impedance higher at all or part of the frequencies that are from the frequency corresponding to DC, to the frequency corresponding to the occupied bandwidth and/or at least one higher harmonic frequency of a carrier wave of the input signal. This is a novel and unobvious difference between Miguelez and applicants' invention as described in claim 1.

As such, Applicants respectfully submit that present independent claim 1, and dependent claims 2, 3, 6, 7 and 9, are not anticipated by Miguelez et al. under 35 U. S. C. § 102.

Applicants further submit that the presently claimed invention is not made obvious by Miguelez, singly or in any combination with Yun and Fukuden. Miguelez fails to teach or suggest the features described above in the presently claimed invention: a) that the specific-frequency means directly is connected to one or both sides of a nonlinear device (without an intervening device), and b) that the specific-frequency suppressing means has an impedance lower than the impedance of the nonlinear device. Applicants courteously point out that the Examiner has incorrectly interpreted claim 11 as a dual amplifier. Claim 11 is an embodiment of the claimed invention including a bipolar transistor 1303 (new Figure 12a), and claim 10 is an embodiment including a FET 1303′ (new Figure 12b). Thus, Applicants submit that Miguelez does not teach or suggest employing the structure as described in claim 1 and dependent claims 2-10. And, neither Yun nor Fukuden remedy the deficiencies of Miguelez with respect to the claimed invention.

Therefore, allegedly combining Miguelez with Yun or Fukuden likewise does not render the claimed invention obvious. Moreover, there is nothing in their cited documents that would have motivated one of ordinary skill in the art to have combined the teachings of the cited art in any way that would render the claimed invention obvious. Hence, the asserted rejections over the alleged combinations of Miguelez, Yun and Fukuden are overcome. Independent claim 1, and the dependent claims thereon, are in condition for allowance.

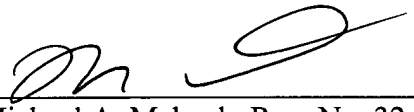
New claims 12-14 were added to further detail the features introduced in claim 1. No new matter was added, and the new claims are supported by the originally submitted specification, drawings and claims. Therefore, new claims 12-14 also should be allowed.

* * * *

Applicants respectfully submit that this Amendment and the above remarks obviate the outstanding rejections and objections in this case, thereby placing the application in condition for immediate allowance. Allowance of this application is earnestly solicited.

If any fees under 37 C. F. R. §§ 1.16 or 1.17 are due in connection with this filing, please charge the fees to Deposit Account No. 02-4300, Order No. 033216M067.

Respectfully submitted,
SMITH, GAMBRELL & RUSSELL, LLP

By: 

Michael A. Makuch, Reg. No. 32,263
1850 M Street, N.W., Suite 800
Washington, D.C. 20036
Telephone: (202) 263-4300
Facsimile: (202) 263-4329

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MARKED UP VERSION OF CHANGES

IN THE SPECIFICATION:

Page 33, first full paragraph:

The scope of the present invention includes a power amplifier comprising: a predistortion circuit described in each above-mentioned embodiment; and an amplifier for amplifying the signal from the predistortion circuit. An example of such an amplifier is shown in [Figure 12] Figures 12a and 12b. Figure 12a describes an amplifier with a bipolar transistor 1303, and Figure 12b replaces the bipolar transistor 1303 with a field-effect transistor (FET) 1303′.

Page 33, last paragraph bridging pages 33 and 34:

The power amplifier input signal composed of: an input terminal 1301 for inputting a signal; a first matching circuit 1302 connected to the input terminal 1301; a transistor 1303, (1303′) the gate of which is connected to the first matching circuit 1302; a second matching circuit 1304 connected to the drain of the transistor 1303, (1303′); an output terminal 1305 connected to the second matching circuit 1304 and for outputting a signal; a first bias circuit 1306 connected between the first matching circuit 1302 and the transistor 1030, (1303′), first specific-frequency suppressing means 1307 connected between the first bias circuit 1306 and the transistor 1303, (1303′) and of suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to the input terminal and/or at least one higher harmonic frequency of the carrier wave of the input signal; a second bias circuit 1308 connected between the second matching circuit 1304 and the transistor 1303, (1303′); and second specific-frequency suppressing means 1309 connected between the second bias circuit 1308 and the transistor 1303,

(1303') and of suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to input terminal and/or at least one higher harmonic frequency of the carrier wave of the input signal.

Page 34, first full paragraph:

As shown in [Figure 12] Figures 12a and 12b, the input side and/or the output side of the transistor 1303, (1303') are provided with specific-frequency suppressing means 1307, 1309 of suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to the input terminal and/or at least one higher harmonic frequency of the carrier wave of the input signal, whereby the unbalance of distortion in the signal generated by the amplifier can also be suppressed. Accordingly, an amplifier shown in [Figure 12 enhances] Figures 12a and 12b enhance the effect of suppressing the overall unbalance of distortion in the signal of a power amplifier. Here, the second bias circuit 1308 may be the circuit shown in Figure 13. When the second bias circuit 1308 is the circuit shown in Figure 13, the second bias circuit 1308 serves as a specific-frequency suppressing means.

IN THE CLAIMS:

1. (Amended) A predistortion circuit comprising:

an input terminal for inputting a predetermined signal;

a nonlinear device directly or indirectly connected to said input terminal;

A bias supply circuit for applying a voltage to said nonlinear device;

specific-frequency suppressing means connected to one side or both sides of said nonlinear device directly without another intervening device [and of] , said specific-frequency

suppressing means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width on in input signal inputted to said input terminal and/or suppressing at lest one higher harmonic frequency of a carrier wave of said input signal; and

an output terminal for outputting a signal.

2. (Amended) A predistortion circuit of Claim 1, wherein said specific-frequency suppressing means has such impedance that the impedance of said specific-frequency suppressing means viewed from the connection point to which said specific-[ ]frequency suppressing means is connected is lower than the impedance of said nonlinear device viewed from said connection point at all or part of such frequencies that are from said frequency corresponding to DC to said frequency corresponding to said occupied band width and/or at least one higher harmonic frequency of a carrier wave of said input signal.

10. (Amended) A power amplifier of Claim 9, wherein said amplifier comprises:

an input terminal for inputting a signal;

a first matching circuit connected to said input terminal;

a transistor the gate of which is connected to said first matching circuit;

a second matching circuit connected to the drain of said transistor;

an output terminal connected to said second matching circuit and for outputting a signal;

a first bias circuit connected between said first matching circuit and said transistor;

a second bias circuit connected between said second matching circuit and said transistor; and

specific-frequency suppressing means connected to one side or both sides of said transistor directly without another intervening device [and of] , said specific-frequency

suppressing means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to said input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of said input signal.

11. (Amended) A power amplifier of Claim 10, wherein said amplifier comprises:

an input terminal for inputting a signal;

a first matching circuit connected to said input terminal;

a transistor the base of which is connected to said first matching circuit;

a second matching circuit connected to the collector of said transistor;

an output terminal connected to said second matching circuit and for outputting a signal;

a first bias circuit connected between said first matching circuit and said transistor;

a second bias circuit connected between said second matching circuit and said transistor; and

specific-frequency suppressing means connected to one side or both sides of said transistor directly without another intervening device [and of] , said specific-frequency suppressing means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to said input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of said input signal.

CLEAN VERSION OF CHANGES

IN THE SPECIFICATION:

Page 33, first full paragraph:

The scope of the present invention includes a power amplifier comprising: a predistortion circuit described in each above-mentioned embodiment; and an amplifier for amplifying the signal from the predistortion circuit. An example of such an amplifier is shown in Figures 12a and 12b. Figure 12a describes an amplifier with a bipolar transistor 1303, and Figure 12b replaces the bipolar transistor 1303 with a field-effect transistor (FET) 1303′.

Page 33, last paragraph bridging pages 33 and 34:

The power amplifier input signal composed of: an input terminal 1301 for inputting a signal; a first matching circuit 1302 connected to the input terminal 1301; a transistor 1303, (1303′) the gate of which is connected to the first matching circuit 1302; a second matching circuit 1304 connected to the drain of the transistor 1303, (1303′); an output terminal 1305 connected to the second matching circuit 1304 and for outputting a signal; a first bias circuit 1306 connected between the first matching circuit 1302 and the transistor 1030, (1303′), first specific-frequency suppressing means 1307 connected between the first bias circuit 1306 and the transistor 1303, (1303′) and of suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to the input terminal and/or at least one higher harmonic frequency of the carrier wave of the input signal; a second bias circuit 1308 connected between the second matching circuit 1304 and the transistor 1303, (1303′); and second specific-frequency suppressing means 1309 connected between the second bias circuit 1308 and the transistor 1303,

(1303′) and of suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to input terminal and/or at least one higher harmonic frequency of the carrier wave of the input signal.

Page 34, first full paragraph:

As shown in Figures 12a and 12b, the input side and/or the output side of the transistor 1303, (1303′) are provided with specific-frequency suppressing means 1307, 1309 of suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to the input terminal and/or at least one higher harmonic frequency of the carrier wave of the input signal, whereby the unbalance of distortion in the signal generated by the amplifier can also be suppressed. Accordingly, an amplifier shown in Figures 12a and 12b enhance the effect of suppressing the overall unbalance of distortion in the signal of a power amplifier. Here, the second bias circuit 1308 may be the circuit shown in Figure 13. When the second bias circuit 1308 is the circuit shown in Figure 13, the second bias circuit 1308 serves as a specific-frequency suppressing means.

IN THE CLAIMS:

1. (Amended) A predistortion circuit comprising:

an input terminal for inputting a predetermined signal;

a nonlinear device directly or indirectly connected to said input terminal;

A bias supply circuit for applying a voltage to said nonlinear device;

specific-frequency suppressing means connected to one side or both sides of said nonlinear device directly without another intervening device, said specific-frequency suppressing

means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width on in input signal inputted to said input terminal and/or suppressing at lest one higher harmonic frequency of a carrier wave of said input signal; and

an output terminal for outputting a signal.

2. (Amended) A predistortion circuit of Claim 1, wherein said specific-frequency suppressing means has such impedance that the impedance of said specific-frequency suppressing means viewed from the connection point to which said specific-frequency suppressing means is connected is lower than the impedance of said nonlinear device viewed from said connection point at all or part of such frequencies that are from said frequency corresponding to DC to said frequency corresponding to said occupied band width and/or at least one higher harmonic frequency of a carrier wave of said input signal.

10. (Amended) A power amplifier of Claim 9, wherein said amplifier comprises:

an input terminal for inputting a signal;

a first matching circuit connected to said input terminal;

a transistor the gate of which is connected to said first matching circuit;

a second matching circuit connected to the drain of said transistor;

an output terminal connected to said second matching circuit and for outputting a signal;

a first bias circuit connected between said first matching circuit and said transistor;

a second bias circuit connected between said second matching circuit and said transistor; and

specific-frequency suppressing means connected to one side or both sides of said transistor directly without another intervening device, said specific-frequency suppressing means

suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to said input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of said input signal.

11. (Amended) A power amplifier of Claim 10, wherein said amplifier comprises:

an input terminal for inputting a signal;

a first matching circuit connected to said input terminal;

a transistor the base of which is connected to said first matching circuit;

a second matching circuit connected to the collector of said transistor;

an output terminal connected to said second matching circuit and for outputting a signal;

a first bias circuit connected between said first matching circuit and said transistor;

a second bias circuit connected between said second matching circuit and said transistor; and

specific-frequency suppressing means connected to one side or both sides of said transistor directly without another intervening device, said specific-frequency suppressing means suppressing all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied band width of an input signal inputted to said input terminal and/or suppressing at least one higher harmonic frequency of a carrier wave of said input signal.

12. (New) A predistortion circuit of claim 6, wherein said specific-frequency suppressing means is composed of lumped parameter components interconnected in series.

13. (New) A predistortion circuit of claim 6, wherein said specific-frequency suppressing means is composed of a transmission line.

14. (New) A predistortion circuit of claim 6, wherein said specific-frequency suppressing means is composed of a transmission line and a capacitor interconnected in series.